Amendm nts to the Claim

Claims 1 to 30 (Cancelled)

31. (New) A loop filter for a phase locked loop ("PLL") circuit which locks a frequency of a signal to a reference frequency, comprising:

a proportional path circuit which receives a charge pump output and determines and holds a charge to be directed to or taken from a PLL circuit throughout an update period based on a detected phase difference for the update period for locking a frequency of a signal for the PLL circuit to a reference frequency and wherein the proportional path circuit provides an independent proportional path output; and

an integral path circuit that is separate and independent from the proportional path circuit wherein the integral path circuit receives another charge pump output and tracks a total charge level for the PLL circuit based on phase differences for present and prior update periods and wherein the integral path circuit provides an independent integral path output; and

a summer that receives and sums the independent proportional path output and the independent integral path output to provide a low-jitter loop filter output.

32. (New) The loop filter according to Claim 31, wherein the proportional path circuit further comprises:

a transconductance stage, which receives as an input the charge pump output, for converting a voltage signal based on the signal to a current signal;

a capacitor that is able to couple to the charge pump output or to a reset voltage level wherein the capacitor is respectively able to be charged to hold the charge and to be reset by discharging to the reset voltage level; and

another capacitor that is able to couple to the charge pump output or to the reset voltage level wherein the another capacitor is also respectively able to be charged to hold the charge and to be reset by discharging to the reset voltage level.

33. (New) The loop filter according to Claim 32, wherein the proportional path circuit further comprises:

a hold switch activated to couple the capacitor to the one charge pump;

a reset switch activated to couple the capacitor to a reset voltage source to set the capacitor to the reset voltage level;

another hold switch activated to couple the another capacitor to the one charge pump; and

another reset switch activated to couple the another capacitor to the reset voltage source to set the another capacitor to the reset voltage level.

34. (New) The loop filter according to Claim 33, wherein the detected phase difference is detected by a phase frequency detector and wherein the phase frequency detector controls activation and deactivation of the hold switch, the reset switch, the another hold switch, and the another reset switch to charge, hold, and reset the capacitor and the another capacitor at appropriate times.

35. (New) The loop filter according to Claim 31, wherein the integral path circuit further comprises a loop filter stage.

36. (New) The loop filter according to Claim 35, wherein the loop filter stage further comprises a capacitor, a transistor, and a resistor wherein the capacitor is coupled between a gate of the transistor and ground, the resistor is coupled between a source of the transistor and ground, and a drain of the transistor is coupled to the summer and wherein the gate of the transistor receives the another charge pump output.

37. A loop filter for a phase locked loop ("PLL") circuit which locks a frequency of a signal to a reference frequency, comprising:

circuit to a reference frequency; and

an integral path circuit that is independent from the proportional path circuit wherein the integral path circuit generates an integral path output that tracks an overall input signal level including prior proportional output signals generated by the proportional path circuit; and

a summer that receives and sums the proportional path output and the integral path output to provide a low-jitter loop filter output.

38. (New) The loop filter according to Claim 37, wherein the proportional path circuit further comprises:

a transconductance stage, which receives as an input a charge pump output, for converting a voltage signal based on the signal to a current signal;

a capacitor that is able to couple to the charge pump output or to a reset voltage level wherein the capacitor is respectively able to be charged to hold the charge and to be reset by discharging to the reset voltage level; and

another capacitor that is able to couple to the charge pump output or to the reset voltage level wherein the another capacitor is also respectively able to be charged to hold the charge and to be reset by discharging to the reset voltage level.

39. (New) The loop filter according to Claim 37, wherein the integral path circuit further comprises a loop filter stage.

40. (New) The loop filter according to Claim 39, wherein the loop filter stage further comprises a capacitor, a transistor, and a resistor wherein the capacitor is coupled between a gate of the transistor and ground, the resistor is coupled between a source of the transistor and ground, and a drain of the transistor is coupled to the summer and wherein the gate of the transistor receives a charge pump output.

41. (New) A method of implementing a loop filter for a phase locked loop ("PLL") circuit which locks a frequency of a signal to a reference frequency, comprising:

separating a proportional path circuit from an integral path circuit so that the proportional path circuit and the integral path circuit are independent from each other;

generating, by the proportional path circuit, a proportional output signal based on a detected instantaneous phase difference for locking a frequency of a signal for the PLL circuit to a reference frequency; and

generating, by the integral path circuit, an integral path output that tracks an overall input signal level including prior proportional output signals generated by the proportional path circuit; and

summing, by a summer, the proportional path output and the integral path output to provide a low-jitter loop filter output.

42. (New) The method according to Claim 41, wherein generating, by the proportional path circuit, a proportional output signal further comprises:

receiving, by a transconductance stage, as an input a charge pump output for converting a voltage signal based on the signal to a current signal;

coupling a capacitor to the charge pump output or to a reset voltage level wherein the capacitor is respectively able to be charged to hold the charge and to be reset by discharging to the reset voltage level; and

coupling another capacitor to the charge pump output or to the reset voltage level wherein the another capacitor is also respectively able to be charged to hold the charge and to be reset by discharging to the reset voltage level.

43. (New) The method according to Claim 41, wherein the integral path circuit further comprises a loop filter stage.

44. (New) The method according to Claim 43, wherein the loop filter stage further comprises a capacitor, a transistor, and a resistor and the capacitor is coupled between a gate of the transistor and ground, the resistor is coupled between a source of the transistor and ground, and a drain of the transistor is coupled to an input of the summer; and

wherein generating, by the integral path circuit, an integral path output further comprises:

receiving a charge pump output through the gate of the transistor and providing the integral path output through the drain of the transistor.